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Gutsche et al.

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(54) **VERTICAL INTERCONNECT STRUCTURE,
MEMORY DEVICE AND ASSOCIATED
PRODUCTION METHOD**

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H01L 27/108 (2006.01)
B82Y 10/00 (2011.01)
H01L 21/768 (2006.01)
H01L 27/22 (2006.01)

(52) **U.S. Cl.**

CPC **H01L 27/24** (2013.01); **H01L 21/28525** (2013.01); **H01L 21/76885** (2013.01); **H01L 21/76889** (2013.01); **H01L 27/10855** (2013.01); **H01L 27/10888** (2013.01); **B82Y 10/00** (2013.01); **H01L 21/76834** (2013.01); **H01L 27/228** (2013.01); **H01L 2221/1094** (2013.01)

(58) **Field of Classification Search**

CPC H01L 27/108–27/10897
USPC 438/630, 649; 257/746, 768–770, 257/E21.589, E51.591, E51.593
See application file for complete search history.

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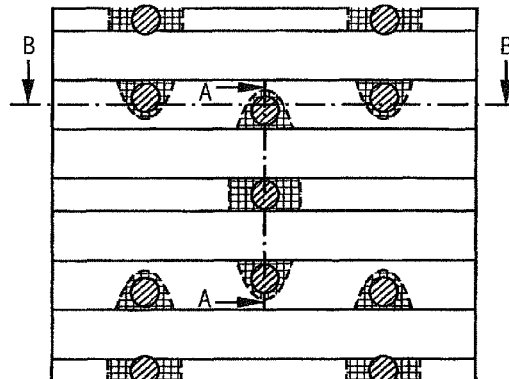
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Assistant Examiner — Ali Naraghi

(57) **ABSTRACT**

The present invention relates to a method for producing a vertical interconnect structure, a memory device and an associated production method, in which case, after the formation of a contact region in a carrier substrate a catalyst is produced on the contact region and a free-standing electrically conductive nanoelement is subsequently formed between the catalyst and the contact region and embedded in a dielectric layer.

12 Claims, 13 Drawing Sheets



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FIG 1A

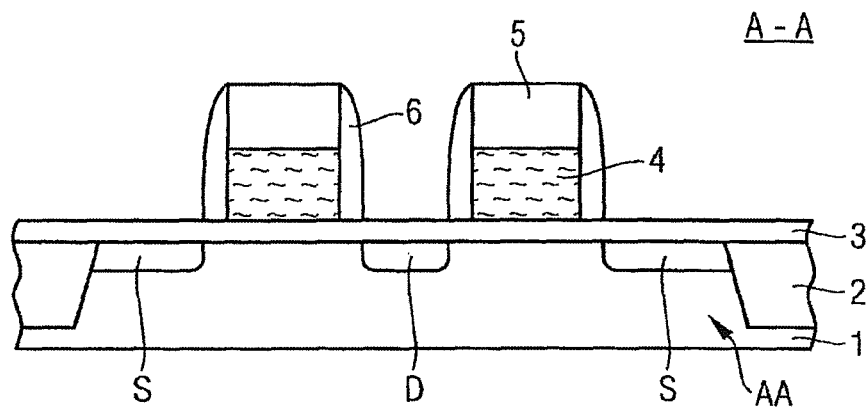


FIG 1B

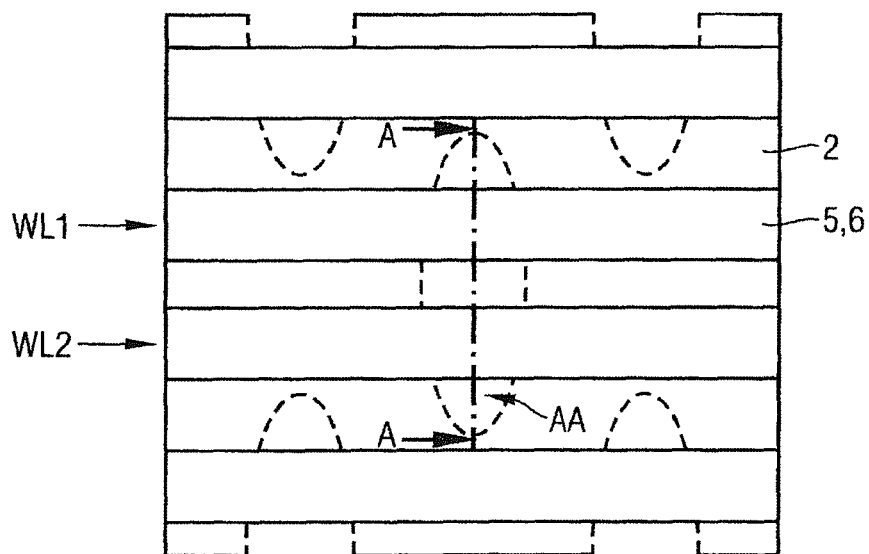


FIG 2

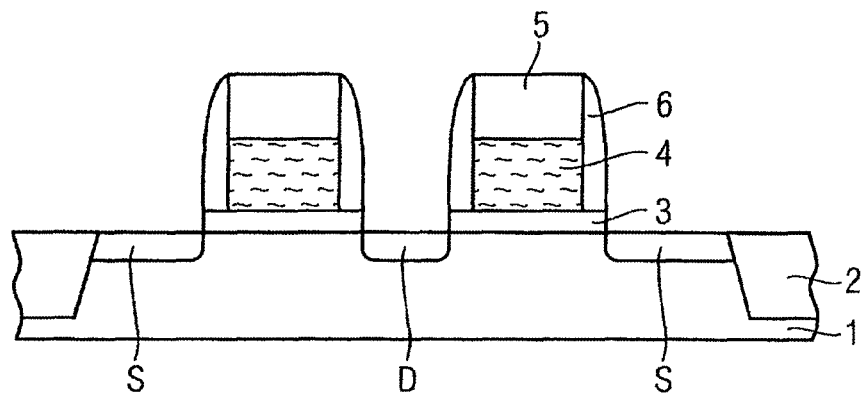


FIG 3

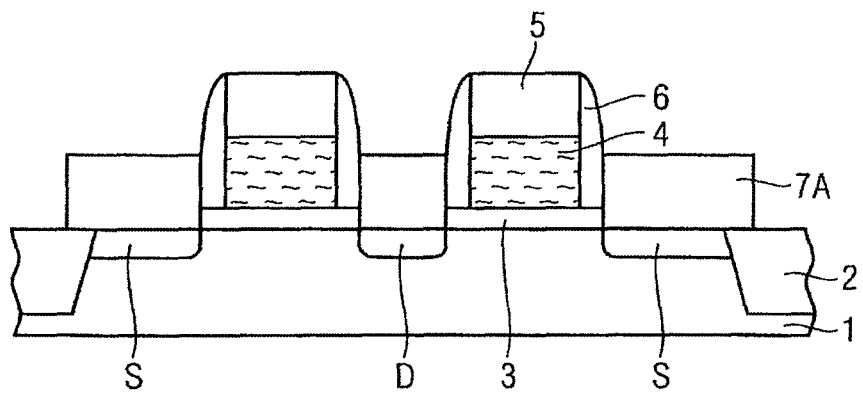


FIG 4

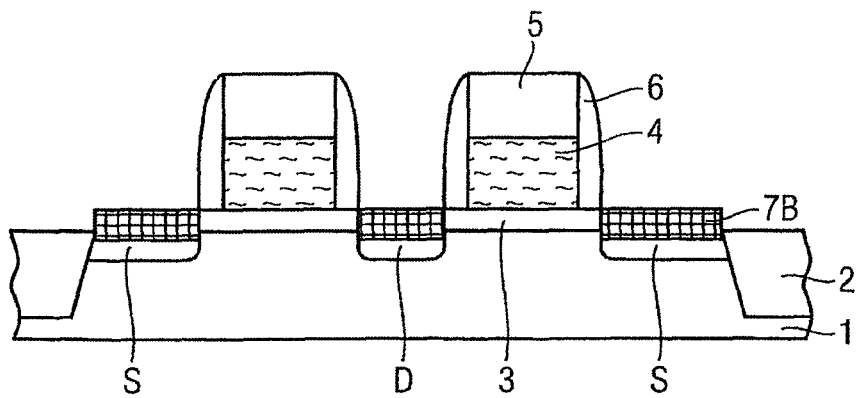


FIG 5A

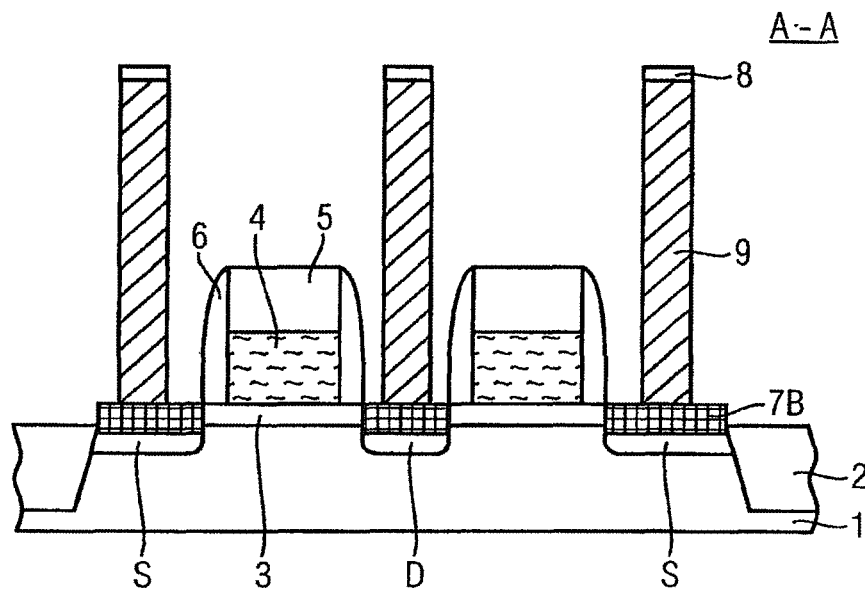


FIG 5B

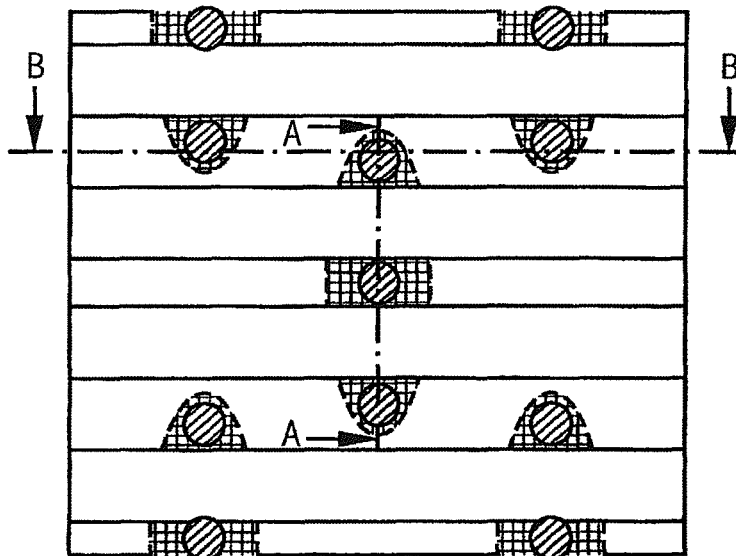


FIG 5C

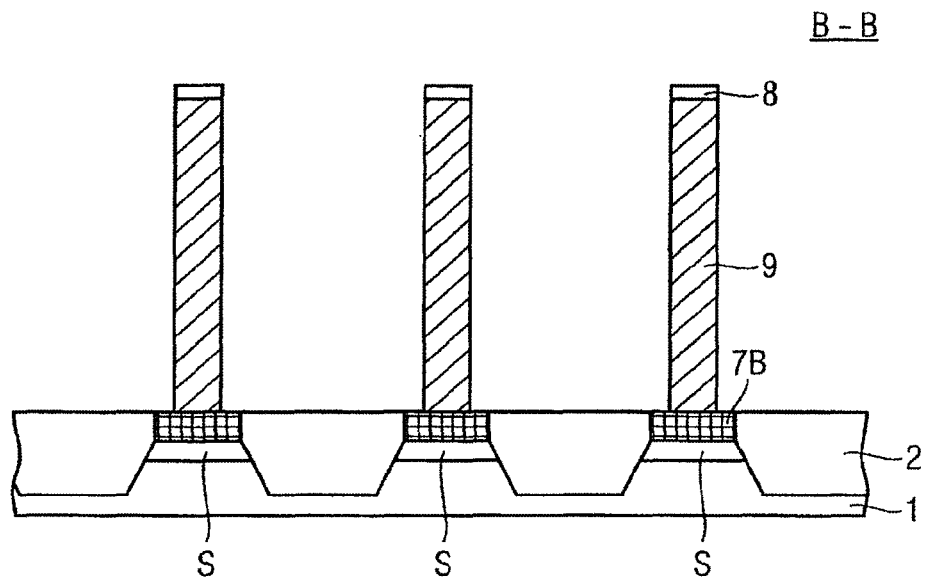


FIG 6

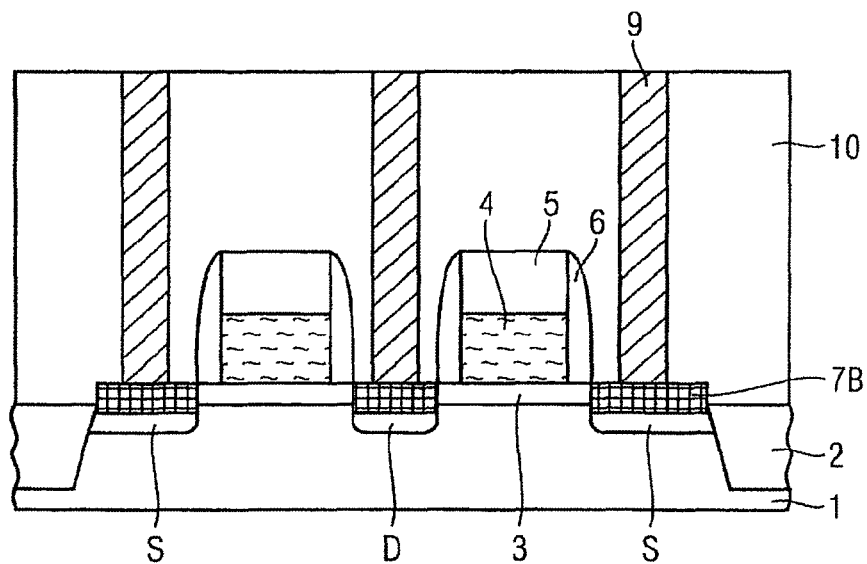


FIG 7

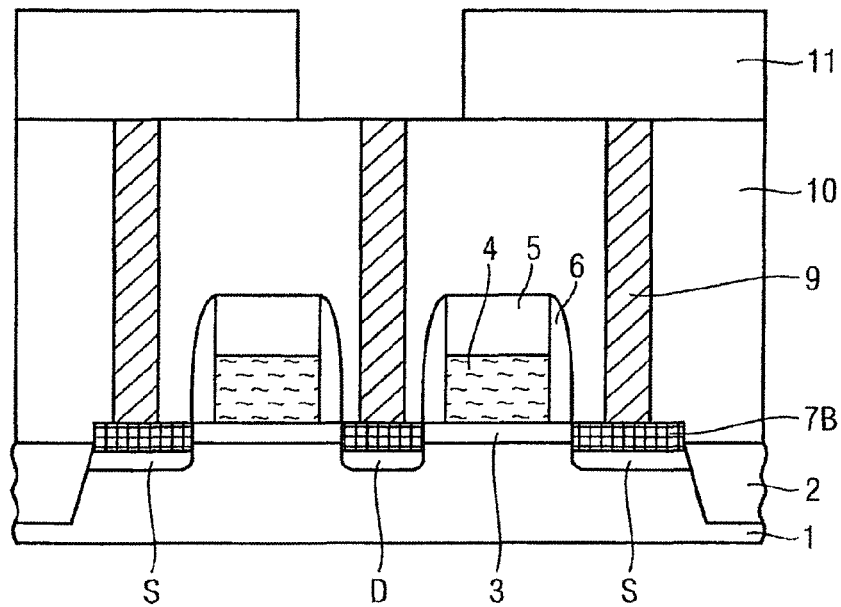


FIG 8A

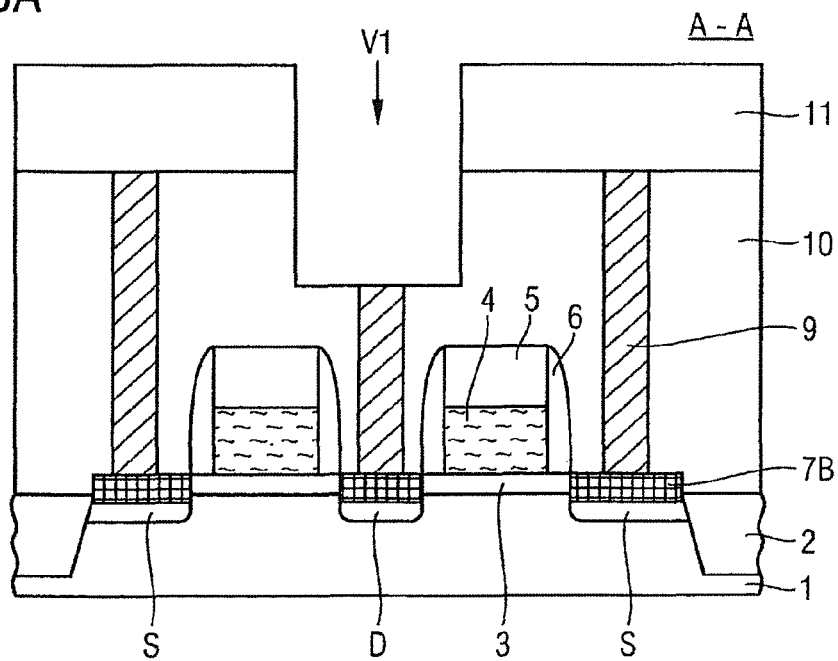


FIG 8B

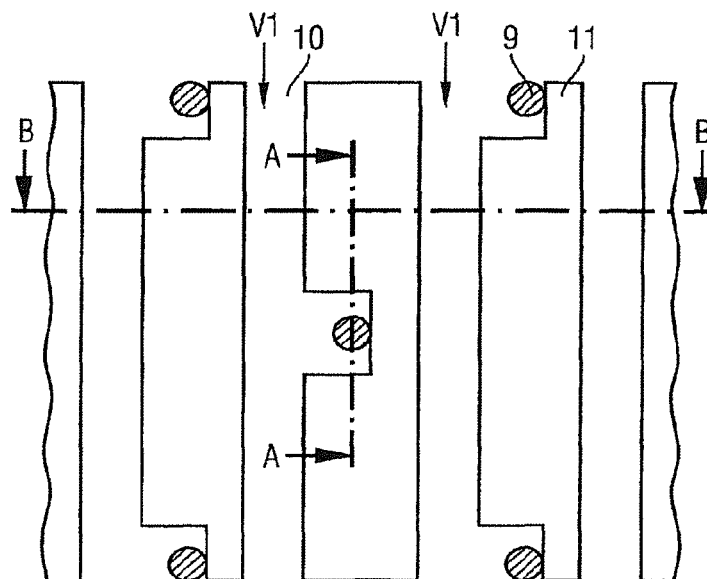


FIG 8C

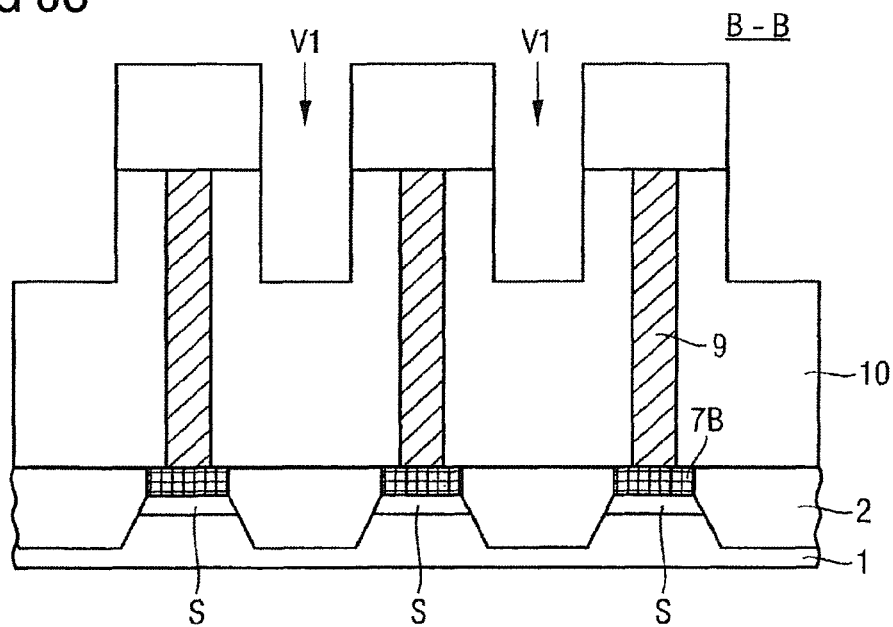


FIG 9A

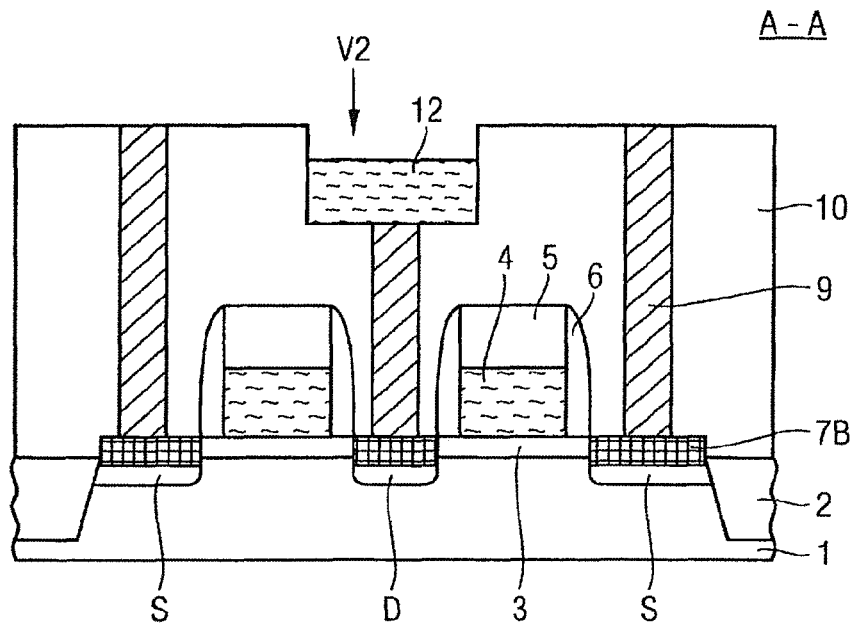
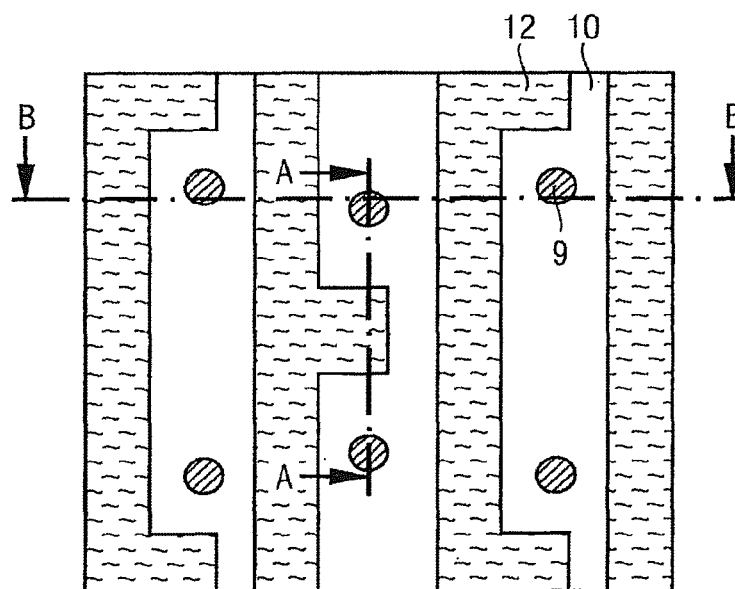


FIG 9B



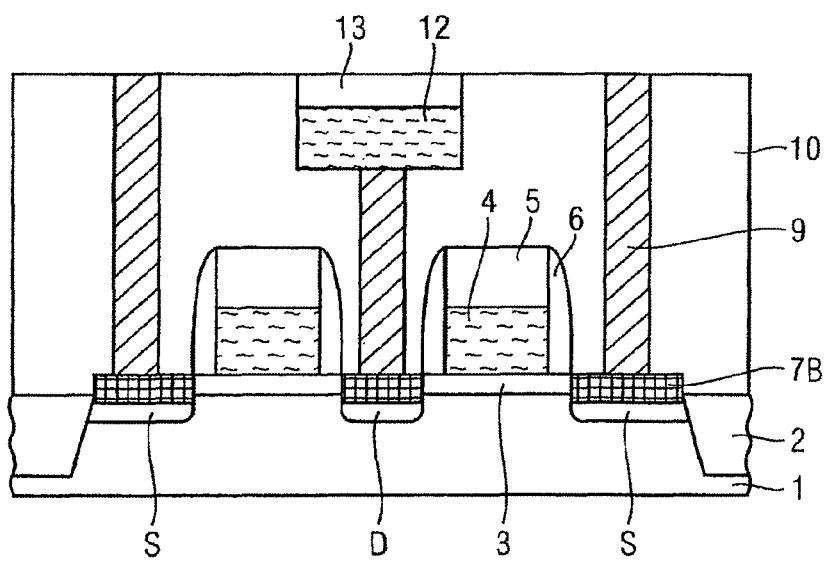


FIG 11

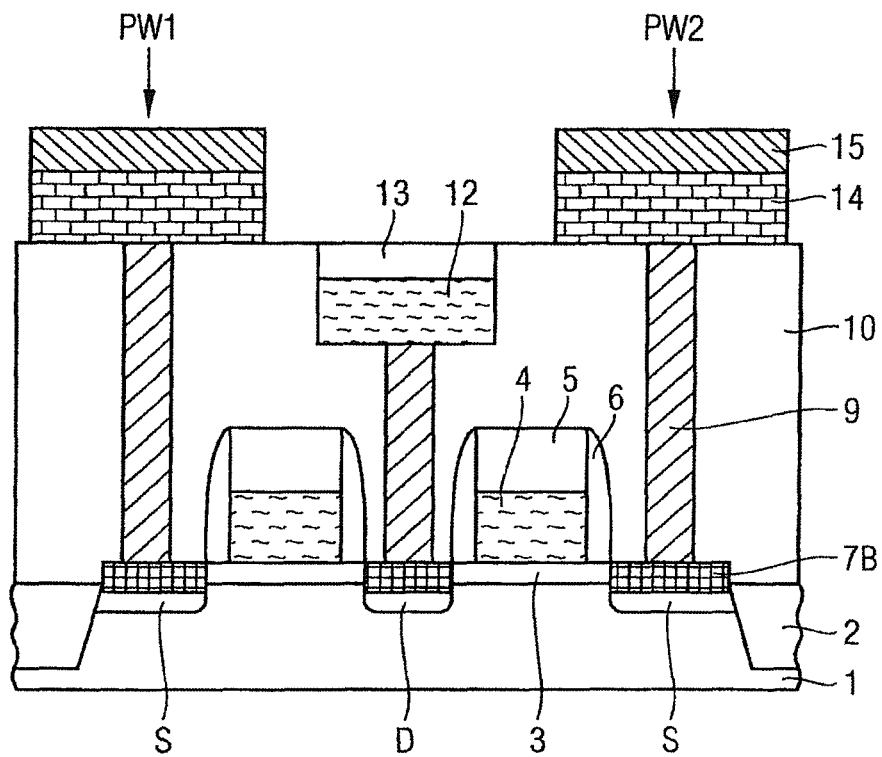


FIG 12A

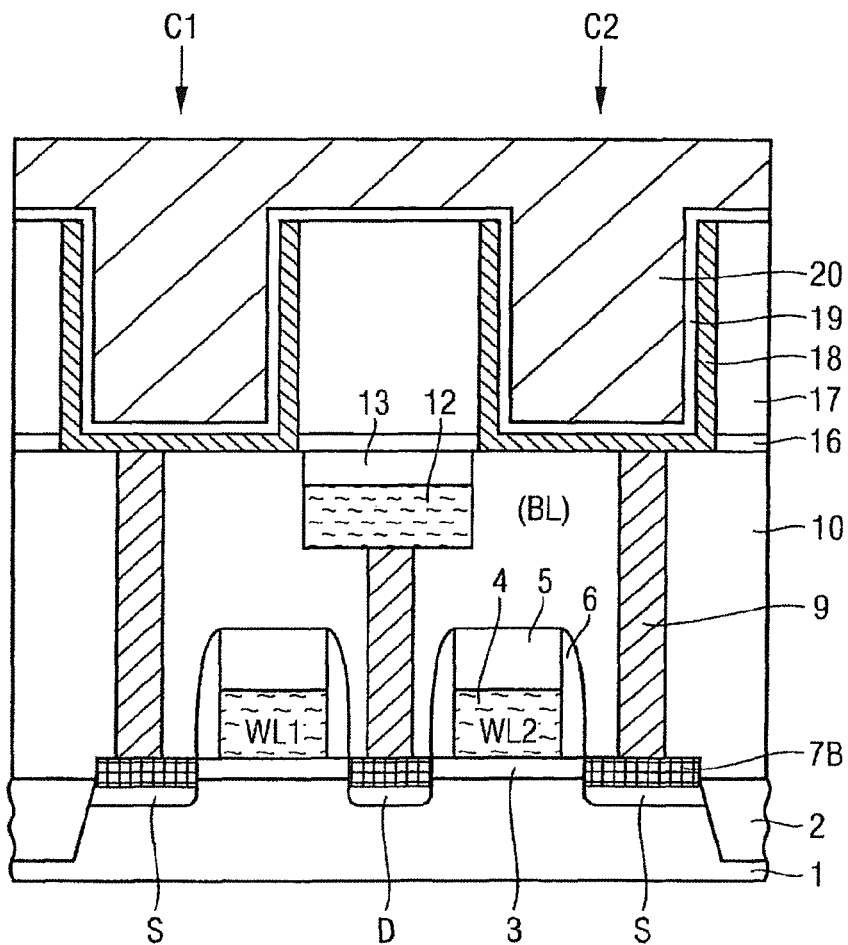


FIG 12B

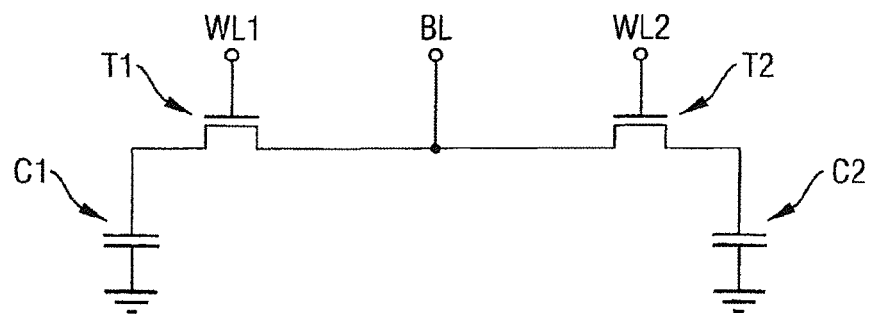


FIG 13A

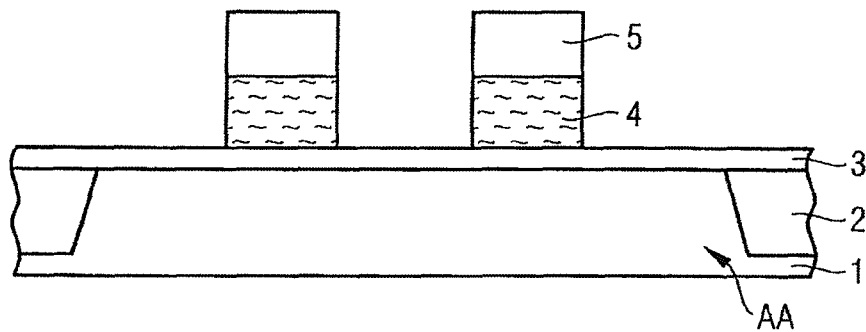


FIG 13B

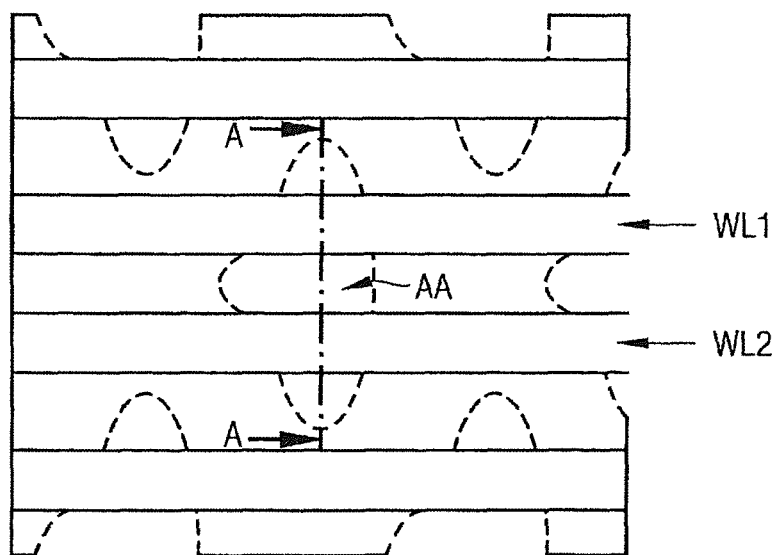


FIG 14

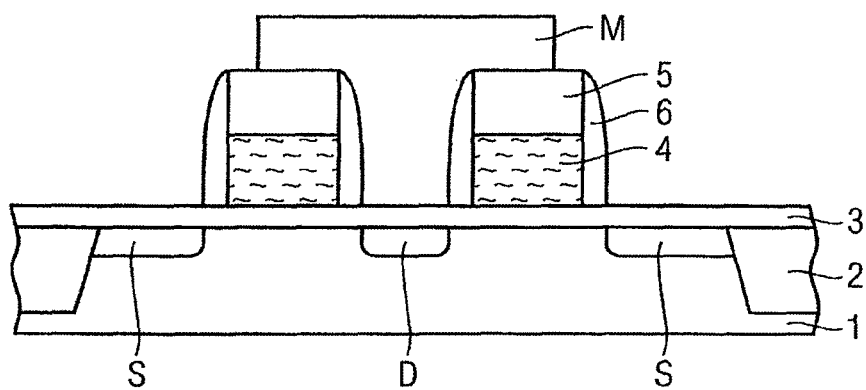
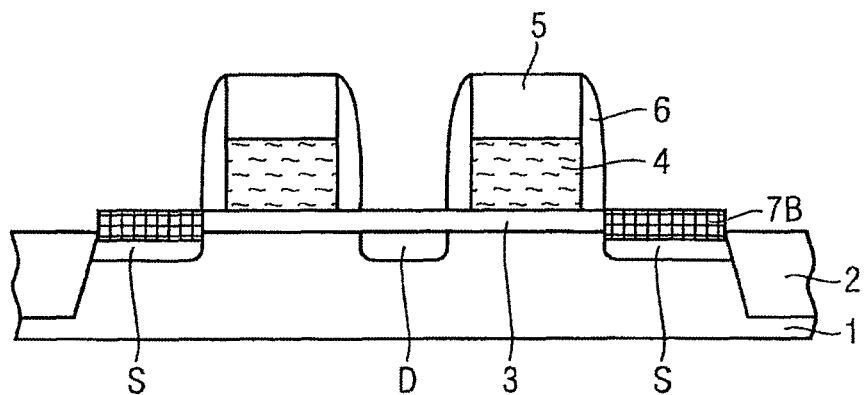
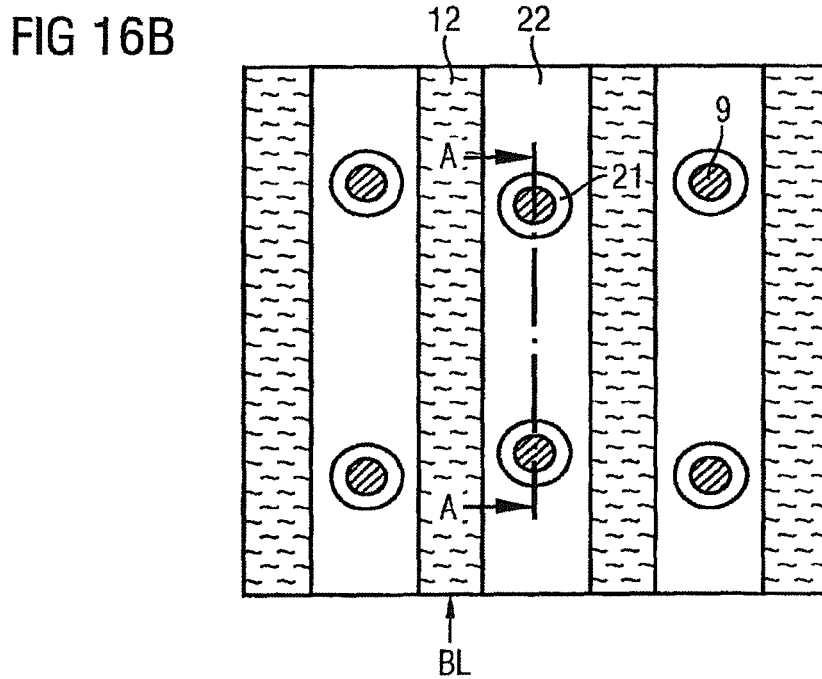
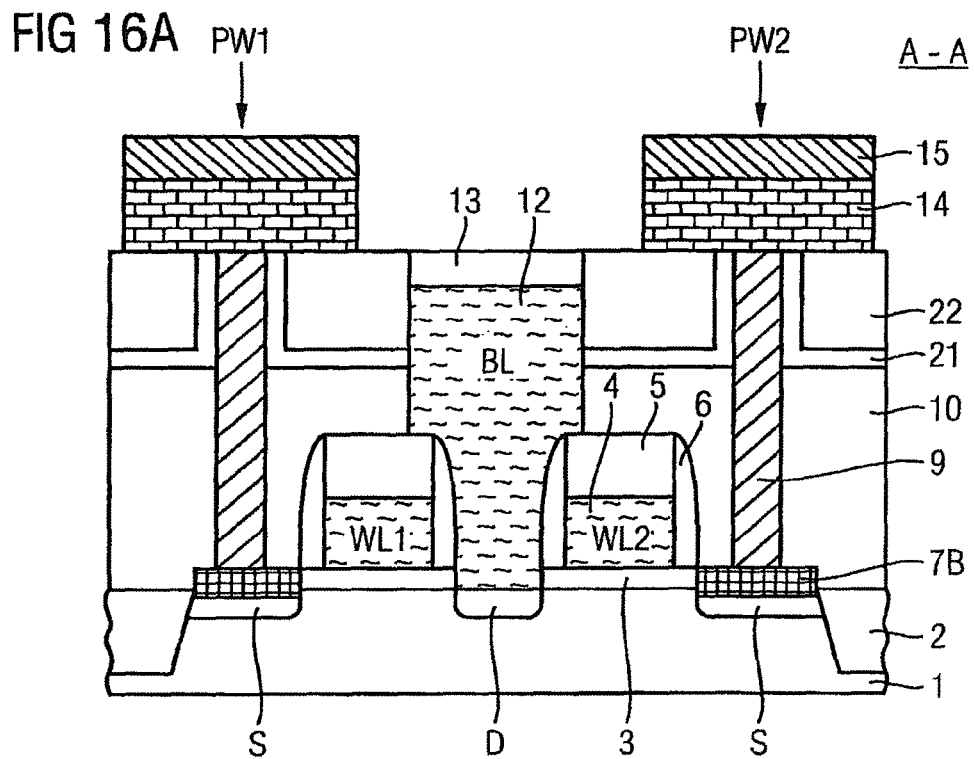


FIG 15





VERTICAL INTERCONNECT STRUCTURE, MEMORY DEVICE AND ASSOCIATED PRODUCTION METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. Ser. No. 13/167,744, filed on Jun. 24, 2011, which is a divisional of U.S. Ser. No. 11/588,769, filed on Oct. 27, 2006, which claims priority to DE 10 2005 051 973.3 filed on Oct. 31, 2005, which are all incorporated herein by reference.

BACKGROUND

1. Field of the Invention

The present invention relates to a vertical interconnect structure, a memory device and an associated production method.

2. Description of Related Art

For the formation of integrated semiconductor circuits, a multiplicity of interconnect structures are required for realizing a wiring or for connecting the semiconductor components formed in the semiconductor substrate. On the one hand, these are horizontal interconnect structures that are formed essentially in metallization planes lying above a semiconductor substrate and are isolated from one another by dielectric layers lying in between. Furthermore, vertical interconnect structures are required, which either enable a contact-connection from a first interconnect or metallization plane to the underlying semiconductor substrate and are usually referred to as contacts or, in superordinate metallization planes or interconnect planes, provide for a connection between said interconnect planes and are usually referred to as contact vias.

Particularly in semiconductor memory devices having volatile or nonvolatile memory elements, a high integration density is necessary in order to realize a maximum number of items of information per unit area. Furthermore, the production costs are of particular importance for commercialization.

Usually, in order to realize such vertical interconnect structures or contacts or contact vias, by means of photolithographic methods, contact holes or openings are formed in the dielectric layers and the contact holes are subsequently filled with electrically conductive filling material. The very high production costs and also the minimum feature sizes which can be realized only to a limited extent, which prevent more extensive integration, are disadvantageous in this case in particular on account of the photolithographic method. Accordingly, there is a need for an improved vertical interconnect structure, memory device and associated methods of production.

SUMMARY

The invention is based on the object of providing a production method for vertical interconnect structures, a memory device and an associated production method, an integration density being increased further and the production costs being reduced further.

In particular, by forming a catalyst on a contact region in a carrier substrate, subsequently forming a free-standing electrically conductive nanoelement between the catalyst and the contact region, and finally embedding the free-standing nanoelement in a dielectric layer, it is possible for the first time to produce vertical interconnect structures with minimal dimensions in self-aligning fashion and thus in a very simple manner.

In order to improve an electrical contact-connection, a metal-semiconductor compound, and particularly when using silicon as semiconductor material so-called silicides, may be formed at the surface of the contact region.

Furthermore, for the purpose of more extensively decreasing or reducing the feature size of the vertical interconnect structure, the catalyst may be coagulated by means of e.g. thermal processing. This results in a self-aligning structure miniaturization process that significantly reduces a cross-sectional area of the vertical interconnect structure.

So-called nanowires, nanotubes or nanofibers are preferably produced as nanoelements or nanostructures. When using silicon nanoelements, a complete siliciding is preferably carried out, whereby the electrical properties of the interconnect structure can be improved further and, in particular, an interconnect resistance is significantly reduced.

As the dielectric layer, SiO₂ is preferably deposited over the whole area by means of e.g. a CVD method and subsequently planarized as far as the surface of the nanoelement. This results in an insulation having outstanding electrical properties, in which case a layer thickness of the dielectric layer can be set particularly simply.

The memory device has at least one memory element and also at least one selection transistor for selecting the at least one memory element via a word line, a bit line furthermore being connected for reading/writing the information. In this case, an electrically conductive and initially free-standing nanoelement connects the memory element to the selection transistor. Memory devices having particularly high integration densities can be formed in this way, with at least one photolithographic mask being saved.

In order to realize so-called elevated source/drain regions, semiconductor layers deposited epitaxially may additionally be formed on the source/drain regions present in the semiconductor substrate, whereby the electrical properties of the selection transistors to be realized can be improved.

Preferably, as the memory element, a phase change memory element is formed at the surface of the dielectric layer and connected via the nanoelement. On account of the very small cross-sectional areas of the nanoelement, the sufficiently high electric current densities required for programming of a phase change material used in phase change memory elements can be realized without any problems.

As an alternative, it is also possible to form capacitors and other resistively switchable memory cells as memory elements at the surface of the dielectric layer embedding the nanoelements.

The memory device preferably has two selection transistors for driving two memory elements, a common diffusion region of the selection transistors electrically connecting the latter to one another. An information density per unit area can be increased further in this way.

With regard to the method for producing a memory device, preferably at least one active region is formed in a semiconductor substrate and strip-type word line stacks with a gate dielectric layer and a gate layer are subsequently formed on the semiconductor substrate or at the surface of the active region in order to define at least two contact regions in the active region. The formation of source/drain regions in said contact regions is followed in turn by formation of at least one free-standing electrically conductive nanoelement on at least one of the contact regions, the at least one free-standing nanoelement subsequently being embedded in a dielectric layer. A bit line layer is furthermore formed at least in the dielectric layer, which is electrically connected to the further contact region. Finally, at least one memory element which is electrically connected to the at least one nanoelement is

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formed at the surface of the dielectric layer. A memory device having extremely high integration density is obtained with minimal costs in this way.

Preferably, a multiplicity of insular active regions are formed in the semiconductor substrate and they are divided into three contact regions by in each case two word line stacks. As a result, two one-transistor memory devices are produced in a cost-effective manner, a contact region that lies between the two word line stacks constituting a common drain region of the selection transistors and respective source regions being realized in the remaining contact regions.

Preferably, a common nanoelement is formed on the common drain region, a first depression subsequently being realized in the dielectric layer in the region of the common nanoelement, a bit line layer being filled into said first depression and the bit line layer subsequently being etched back in order to form a second depression, in order finally to completely fill the second depression with a dielectric filling material. In this way, it is possible to realize a bit line which is completely embedded in the dielectric layer and significantly simplifies subsequent processing and in particular production of the memory elements.

As an alternative, however, it is also possible for no nanoelement to be formed on the common drain region, in which case, after the embedding of the free-standing nanoelements, etching back of the dielectric layer is carried out in order to uncover an upper region of the nanoelements, formation of a dielectric etching stop layer at the surface of the dielectric layer and of the uncovered regions of the nanoelements is carried out, and an auxiliary dielectric layer is formed at the surface of the etching stop layer. Afterward, in the region of the common drain region, a trench is formed in the dielectric layer, the etching stop layer and the auxiliary dielectric layer as far as the drain region, said trench is filled with the bit line layer, the bit line layer is etched back in order to form a depression and said depression is completely filled with dielectric filling material. This again results in a bit line which is completely embedded in the dielectric layer and significantly simplifies subsequent formation of the memory elements.

Further objects, features and advantages of this invention will become readily apparent to persons skilled in the art after a review of the following description, with reference to the drawings and claims that are appended to and form a part of this specification.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1A to 11 illustrate simplified sectional views and also plan views of essential method steps in the production of a memory device with an interconnect structure according to the invention in accordance with a first exemplary embodiment;

FIGS. 12A and 12B show a simplified sectional view and also an associated equivalent circuit diagram of a memory device in accordance with a second exemplary embodiment; and

FIGS. 13A to 16B show simplified sectional views and also plan views for illustrating essential method steps in the production of a memory device in accordance with a third exemplary embodiment.

DETAILED DESCRIPTION

FIGS. 1A and 1B, respectively, show a simplified sectional view and also an associated plan view for illustrating preparatory method steps in the production of a vertical intercon-

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nect structure and a corresponding memory device. First, active regions AA are produced in a carrier substrate 1, which constitutes for example a semiconductor substrate and in particular a monocrystalline silicon semiconductor substrate, by the formation of e.g. a shallow trench isolation 2. The active regions AA are preferably defined in insular fashion, that is to say in the form of oval or rectangular closed-off regions, by means of an STI method (Shallow Trench Isolation).

Afterward, in accordance with FIG. 1A, a gate dielectric layer 3 may preferably be formed over the whole area at the surface of the carrier substrate 1 or of the active regions AA and the shallow trench isolation 2. Preferably, a gate oxide having a high quality and a very small thickness is formed thermally as the gate dielectric layer 3 by means of a thermal oxidation method. Afterward, an electrically conductive gate layer 4 is preferably deposited over the whole area, preferably doped polycrystalline semiconductor material and in particular polysilicon being deposited. Furthermore, a hard mask layer 5 is in turn preferably formed over the whole area at the surface of the gate layer 4, for example silicon nitride or silicon dioxide being used.

Afterward, the gate layer 4 and the hard mask layer 5 are patterned using a resist (not illustrated) by means of photolithographic methods and the word line stacks illustrated in FIG. 1A are formed. In this case, the gate dielectric layer 3 preferably still remains over the whole area. After the removal of the resist (not illustrated), so-called spacers 6 are subsequently formed, e.g. an SiN or SiO₂ layer being deposited over the whole area and etched back anisotropically until only the spacers 6 remain on the sidewalls of the word line stacks.

Using these word line stacks or the additionally present spacers 6 and hard mask layer 5, the corresponding source/drain, connection or LDD implantations can subsequently be carried out for the purpose of realizing the doping regions necessary for a field effect transistor. On account of the insular formation of the active regions AA and the use of precisely two strip-type word line stacks which overlie the active regions AA in such a way that precisely three contact regions are defined in the active region AA, a memory device having two memory cells is obtained in which each memory cell respectively has a field effect transistor and the two memory cells have a common drain contact. A very high integration density is obtained if only for this reason.

FIG. 1B shows a simplified plan view of the illustration in accordance with FIG. 1A, but the illustration of the gate dielectric layer 3 has been omitted here in order to better illustrate the insular structure of the active regions AA in conjunction with the overlying word line stacks or word lines WL1, WL2.

In accordance with FIG. 2, the gate dielectric layer 3 is now removed at least from the surface of the active regions AA or of the semiconductor substrate 1. For this purpose, dilute hydrofluoric acid (HF) is preferably used for the removal of the SiO₂ gate dielectric layer 3.

In an optional method step in accordance with FIG. 3, a so-called elevated source/drain region may subsequently be formed in order to improve the electrical properties of the field effect transistor to be formed, an elevated semiconductor layer 7A being formed at least at a surface of the source/drain regions S and D by means of selective epitaxial deposition methods. A selective Si epitaxy is preferably carried out in this case.

Preferably in accordance with FIG. 4, in addition to the method step in accordance with FIG. 3 or as an alternative thereto, a metal-semiconductor compound 7B may be formed as the surface of the contact regions, in particular self-align-

ing siliciding processes being employed when silicon is used as semiconductor material (salicide, self-aligned silicide). Examples of metal-semiconductor compounds 7B of this type are CoSi, NiSi, TiSi, etc.

In order to form a selective CoSi_x metal-semiconductor compounds 7B, firstly a Co/TiN layer stack may be deposited for example by means of conventional sputtering methods (PVD, Physical Vapor Deposition). This is followed by a first thermal annealing at approximately 500 to 600 degrees Celsius with subsequent wet etching of the residual Co and TiN layers by means of e.g. H₂O₂. Finally, a second thermal annealing of the CoSi metal-semiconductor compound 7B at approximately 600 to 700 degrees Celsius is effected, whereby the metal-semiconductor compound 7B illustrated in FIG. 4 is obtained exclusively at the uncovered surfaces of the semiconductor substrate 1 or the contact regions for the memory device.

In this case, blocking masks may be formed in the periphery of a semiconductor component or of an integrated semiconductor circuit in order to prevent such siliciding.

In accordance with FIGS. 5A to 5C, the vertical interconnect structures are now produced at the surface of the contact regions or of the metal-semiconductor compounds 7B formed at the source and drain regions S and D. In order to avoid processing of edge regions, the latter or a corresponding periphery may once again be covered e.g. by means of a resist.

A respective catalyst is now formed selectively at the uncovered contact regions or at the surface of the metal-semiconductor compounds 7B, e.g. an electroless deposition method being carried out. By way of example, Ti, Pd, Pt, Au, Cu, Co, Cr, Hf, Ir, Mn, Mo, Ni, Rh, Ta, W, or Zr is deposited by means of an electroless deposition method only at the surfaces of the silicided source and drain regions S and D.

If a resist was used for masking in edge regions or at other locations of the semiconductor substrate 1, it can now be stripped or removed. Furthermore, the catalyst 8 may subsequently be coagulated for the purpose of further decreasing a cross-sectional area of the vertical interconnect structure to be formed. To put it more precisely, at a temperature of e.g. 200-500 degrees Celsius the catalyst is liquefied in such a way that catalyst droplets form at the surface of the metal-semiconductor compound 7B, which have a smaller area than the surface areas of said metal-semiconductor compounds 7B. A subsequent step there involves the formation of a free-standing electrically conductive nanoelement or a free-standing electrically conductive nanostructure 9 between the catalyst 8 and the contact region or silicided source and drain region S and D.

Hereinafter the nanoelements or nanostructures 9 formed are, in particular, nanowires, nanotubes or nanofibers, which are acquiring increasing importance in semiconductor technology. The literature reference Lieber, C. M. et al.: "Nanowire Superlattices", Nano Letters, Volume 2, No. 2, February 2002, discloses for example the production of such nanowires with modulated structures. Furthermore, the literature reference Cui, Y. et al.: "High Performance Silicon Nanowire Field Effect Transistors", Nano Letters, Volume 3, No. 2, 2003, pages 149-152, describes the use of silicon nanowires and carbon nanotubes in the production of field effect transistors. Furthermore, the literature reference Cui, Y., et al.: "Diameter-controlled synthesis of single-crystal silicon nanowires", Applied Physics Letters, Volume 78, No. 15, 9 Apr. 2001, pages 2214 to 2216, describes the use of silicon nanowires and the production thereof. Finally, the literature reference Merkulov, V., et al.: "Effects of spatial separation on the growth of vertically aligned carbon nanofibers produced by plasma-enhanced chemical vapor deposition", Applied Phys-

ics Letters, Volume 80, No. 3, 21 Jan. 2002, pages 476-478, discloses the production of vertical carbon nanofibers using an Ni catalyst.

Using one of the methods described above, the free-standing electrically conductive nanoelements or nanostructures 9 illustrated in FIGS. 5A to 5C are now formed in such a way that their height projects significantly above the height of the word line stacks with their hard mask layer 5 and the spacers 6. The free-standing electrically conductive nanoelements 9 are thus formed in a self-aligning manner and without the use of an additional lithography between the catalysts 8 and the contact regions or the source and drain regions S and D.

Optionally, said free-standing electrically conductive nanoelements 9, if semiconductor nanoelements and in particular silicon nanoelements are involved, may subsequently be silicided, whereby an electrical conductivity is significantly increased and the electrical properties of the vertical interconnect structure are thus greatly improved. To put it more precisely, it is possible, once again using a blocking mask in the periphery or at parts of the semiconductor substrate which have to be protected, to apply e.g. a Co/TiN layer stack by sputtering, in which case, as in the case of the metal-semiconductor compound 7B, a first CoSi heat treatment is subsequently carried out, the remaining Co and TiN layers are subsequently subjected to wet etching or removed, and a second CoSi annealing is finally carried out. Preferably, the entire free-standing nanoelement 9 is completely silicided in this case. It goes without saying that other metals, such as Ni for example, are also possible for siliciding, a nickel silicide being formed for the silicon nanoelement 9.

In the—not illustrated—edge regions or connection regions for the word line stacks, corresponding word line contact regions are, of course, firstly covered in order to reliably prevent an undesirable formation of nanoelements. Said word line stacks are usually contact-connected in a conventional manner by means of photolithographic patterning processes, corresponding contact holes being etched free and electrically conductive filling material subsequently being introduced.

In accordance with FIG. 6, the free-standing nanoelements 9 are now completely embedded in a dielectric layer 10, preferably a whole-area deposition of SiO₂ being carried out with subsequent planarization by means of a CMP method which is stopped at the surface or upon reaching the topmost regions of the nanoelements 9. In this way, the free-standing nanoelements 9 can be mechanically stabilized and insulated from one another with a high-quality dielectric material, whereby the electrical and mechanical properties of a semiconductor component are improved. On account of the CMP planarization method used, the catalysts 8, which are no longer required, are simultaneously removed automatically and cost-effectively.

A CVD method (Chemical Vapor Deposition) is preferably used for depositing the dielectric layer 10, in which case the material may have TEOS, in particular.

In accordance with FIG. 7, a further resist layer 11 is applied and patterned photolithographically at the planarized surface of the dielectric layer 10 or of the nanoelements 9. In order to form a bit line, in this case a first depression V1 is etched in the dielectric layer 10 in the region of the common nanoelement 9 formed above the common drain region D, the nanoelement or the nanostructure 9 also being removed at the same time. FIG. 8B illustrates a corresponding plan view, FIG. 8C in turn illustrating a sectional view in accordance with the section B-B.

After this formation of the first depression V1 or the etching of the dielectric layer 10 and the upper region of the

nanoelement 9 for the common drain region D, in accordance with FIGS. 9A to 9C the resist is subsequently removed and the first depression V1 is filled with a bit line layer 12 and the bit line layer 12 is subsequently etched back again in order to form a second depression V2. Doped polycrystalline semiconductor material, and in particular polysilicon, is preferably used as material for the bit line or the bit line layer 12. In principle, however, it is also possible to use metallic materials, and in particular tungsten, as the bit line layer 12.

Afterward, in accordance with FIG. 10, the second depression V2 is completely filled with a dielectric filling material 13, thus resulting in a bit line layer 12 or bit line which is completely embedded in the dielectric layer 10 and is connected to the common drain region D via a common nanoelement 9. Preferably, as the dielectric filling material 13, SiO₂ is once again deposited over the whole area by means of a CVD method and a renewed planarization method is carried out, the upper regions of the further nanoelements 9 serving as stop layers.

In accordance with FIG. 11, the memory elements are now formed at the planarized surface of the dielectric layer or of the uncovered nanoelements 9, so-called phase change memory elements PW1 and PW2 being formed in accordance with the first exemplary embodiment.

Such phase change memory elements use materials which, with regard to their electrical properties, are capable of changing over reversibly from one phase to another phase. By way of example, such materials change between a phase ordered in amorphous fashion and a phase ordered in crystalline or polycrystalline fashion. In particular a resistance or a conductance of such a material differs greatly in these two difference phase states.

Therefore, phase change memory elements usually use such phase change materials, which for example constitute alloys of elements in group VI of the periodic table and are referred to as so-called chalcogenides or chalcogenide materials. Accordingly, such phase change materials are understood hereinafter to be materials which can be changed over between two different phase states having different electrical properties (resistances).

Currently the most widespread chalcogenides or phase change materials comprise an alloy of Ge, Sb and Te (GST, Ge_xSb_yTe_z). Ge₂Sb₂Te₅ is already used in a large number of phase change memory elements and is furthermore known as a material for rewritable optical storage media (e.g. CDs, DVDs, etc.).

The changes in the resistance of phase change materials are utilized in order, for example, to create nonvolatile memory devices (NVM, Non Volatile Memory) and to store information. Accordingly, such materials have a higher resistance in the amorphous phase than in the crystalline or polycrystalline phase. Accordingly, a phase change material may be used as a programmable resistor, the resistance magnitude of which can be reversibly altered depending on its phase state.

An overview of such phase change materials is disclosed for example in the literature reference S. Hatkins et al.: "Overview of phase-change chalcogenide non-volatile memory technology", MRS Bulletin/November 2004, pages 829-832.

A change in the phase in such materials may be caused by a local increase in a temperature. Both phase states are usually stable below 150 degrees Celsius. Above 300 degrees Celsius, rapid crystal nucleation takes place, resulting in a change in the phase state to a crystalline or polycrystalline state, provided that such a temperature is present for a sufficient length of time. To return the phase state to the amorphous state, the temperature is increased to above the melting point of 600 degrees Celsius, followed by very rapid cooling. Both critical

temperatures, i.e. both for the crystallization and for the melting, can be generated using an electric current which flows through an electrically conductive connection electrode with a predetermined resistance and is in contact with or in the vicinity of the phase change material. The heating is in this case carried out by so-called Joule heating.

In accordance with FIG. 11, such a phase change material 14 is now deposited over the whole area at the planarized surface or the nanoelements 9, a PVD or CVD method preferably being carried out. Afterward, a phase change electrode layer 15 is once again preferably deposited over the whole area at the surface of the phase change material layer 14, TiN being deposited, for example. Finally, this layer stack is patterned using conventional photolithographic methods, whereby the phase change memory elements PW1 and PW2 illustrated in FIG. 11 can be realized at the surface regions of the nanoelements.

Whereas the very high programming currents required, which are necessary for the change in the phase state, constitute a significant disadvantage in conventional phase change memory elements, for the first time and without additional costs it is possible, on account of the nanoelements 9 used, to realize very small contact areas to the phase change memory element, which enable the current path to be spatially delimited to a great extent and thus enable the phase change memory elements PW1 and PW2 to be programmed even with very small programming currents. This results in a non-volatile memory device with an extremely high integration density which can be produced extremely cost-effectively and can be operated with very low programming currents.

Further resistively switchable memory elements may also be used besides the phase change memory element described above. They include MRAM memory elements (Magnetic RAM), for example, in which a magnetic layer can be programmed for storing items of information and be read. Furthermore, CBRAM memory elements (Conductive Bridging RAM) are known, for example, in which a conductivity can be set in a solid electrolyte or chalcogenide by producing conductive microbridges. The literature reference G. Müller et al.: "Status and Outlook of Emerging Nonvolatile Memory Technologies", IEEE 2004, describes corresponding memory elements.

FIGS. 12A and 12B show a simplified sectional view of a memory device in accordance with a second exemplary embodiment, stacked capacitors C1 and C2 being used as volatile memory elements instead of the phase change memory elements. In this case, identical reference symbols designate layers and elements identical or corresponding to those in FIGS. 1 to 11, for which reason a repeated description is dispensed with below.

In accordance with the equivalent circuit diagram according to FIG. 12B, the memory device according to the invention thus has two selection transistors T1 and T2, which are respectively connected to a word line WL1 and WL2 and the common drain of which is connected to a common bit line BL. As memory elements, the capacitors C1 and C2 are connected to the respective source regions of the selection transistors T1 and T2, which preferably comprise field effect transistors.

The same method steps as illustrated in FIGS. 1 to 10 are once again carried out in accordance with the second exemplary embodiment, for which reason the detailed description of said method steps is dispensed with below. According to a method step as is illustrated in FIG. 10, in accordance with the second exemplary embodiment firstly an etching stop layer 16 is formed over the whole area, a thin SiN etching stop layer being deposited by means of a CVD method, by way of

example. A further dielectric layer **17** is subsequently formed at the surface of said etching stop layer **16**, an SiO₂ layer preferably again being deposited by means of a CVD method.

Using a resist (not illustrated), a trench or depressions is or are subsequently formed into said further dielectric layer **17** as far as the surface of the dielectric layer **10** at least in the region of the further nanoelements **9** for the source regions S, the further nanoelements **9** being uncovered at their upper surface.

A first capacitor electrode layer **18** is subsequently formed at least at the bottom of the trench surface or the depressions, preferably a polycrystalline semiconductor layer and in particular doped polysilicon being deposited by means of a CVD or ALD (Atomic Layer Deposition) method and being patterned by means of a CMP method. As an alternative, a metal layer such as e.g. TiN may also be used as the first electrode. A capacitor dielectric layer **19** is subsequently formed at least at the surface of the first capacitor electrode layer **18**, a so-called high-k dielectric (e.g. Al₂O₃) preferably being deposited over the whole area by means of ALD methods. Finally, a second capacitor electrode layer **20** or the capacitor counter-electrode is deposited over the whole area, a TiN layer preferably being deposited by means of a CVD or ALD method.

The memory device in accordance with a second exemplary embodiment as illustrated in FIG. **12A** is obtained in this way, which once again has a high integration density and can be produced in a particularly cost-effective manner. The significant cost advantages arise in particular on account of the vertical interconnect structures which are grown in a self-aligning manner at the surface of the source and drain regions S and D.

Furthermore, it is also possible to use capacitors as non-volatile memory elements, the capacitor dielectric comprising e.g. a ferroelectric material, e.g. PZT (lead zirconium titanate). Memory elements of this type are usually referred to as FeRAM memory elements (ferroelectric RAM). The literature reference G. Müller et al.: "Status and Outlook of Emerging Nonvolatile Memory Technologies", IEEE 2004, describes corresponding memory elements.

FIGS. **13A** to **16B** show further sectional views and also plan views for illustrating essential method steps in the production of a memory device in accordance with a third exemplary embodiment, identical reference symbols designating elements identical or corresponding to those in FIGS. **1** to **12**, for which reason a repeated description is dispensed with below.

In accordance with FIGS. **13A** and **13B**, firstly insular active regions AA are once again formed at the surface of the carrier substrate **1** by means of an STI method and strip-type word line stacks or word lines WL1 and WL2 are arranged there above. In contrast to the first and second exemplary embodiments, however, the active region AA has a laterally protruding projection in its central region, in which a common drain region D will be formed later, said projection being provided for direct contact-connection of the common drain region D by a bit line layer that is to be formed later.

In accordance with FIG. **14**, in this case, after forming the spacers **6** and carrying out the various implantations for forming the source and drain regions S and B, a drain mask M is preferably formed in strip-type fashion between the word line stacks WL1 and WL2 for the purpose of covering at least the common drain region D.

Preferably, a so-called SiLK is in this case deposited over the whole area and patterned in accordance with FIG. **14**, reference being made in particular to the literature reference A. Birner et al.: "A fourth material: Thermally stable organic

gap-fill spin-on-polymer enabling new integration concepts", IEDM Tech. Dig., December 2003, pages 665 to 668. This mask layer M, which is also used as a blocking mask for later siliciding, may likewise be formed in the edge regions or the periphery of a respective semiconductor circuit.

In accordance with FIG. **15**, after the removal of the gate dielectric layer **3** at the uncovered surfaces of the carrier substrate **1** using, for example, dilute hydrofluoric acid (HF), a metal-semiconductor compound **7B** is once again implemented at the uncovered contact regions or at the uncovered source regions S, in which case it is possible to form e.g. CoSi_x as metal-semiconductor compound **7B**. Reference is made here to the comparable process steps in accordance with the first and second exemplary embodiments.

Preferably, however, prior to the second CoSi annealing step, the SiLK mask is removed selectively with respect to the SiO₂ and Si₃N₄ and the second annealing step is then carried out. Afterward, the same steps as in FIGS. **5** and **6** are once again carried out, but after the planarization step as far as the upper surfaces of the nanoelements **9** in accordance with FIG. **6**, now the dielectric layer **10** is etched back in order to uncover an upper region of the nanoelements **9** and a dielectric etching stop layer **21** is subsequently formed at the surface of the dielectric layer **10** and the uncovered regions of the nanoelements **9**.

Preferably Si₃N₄ is once again deposited over the whole area as the dielectric etching stop layer **21**. An auxiliary dielectric layer **22** is subsequently formed over the whole area at the surface of the etching stop layer **21**, an SiO₂ deposition with subsequent planarization preferably being carried out.

In order to form the bit line, in the region of the common drain region D, a trench is subsequently formed in the dielectric layer **10**, the etching stop layer **21** and the auxiliary dielectric layer **22** down to the drain region D and the trench is firstly completely filled with the bit line layer **12**. Preferably polycrystalline semiconductor materials, and in particular doped polysilicon, are once again used as materials for the bit line layer **12**. In principle, however, it is also possible to use metallic materials, and in particular tungsten.

The bit line layer **12** is once again etched back in its upper region in order to form a further depression and the further depression is finally filled completely with the dielectric filling material **13**. In this case, materials comparable to those in the first or second exemplary embodiment are once again used and a whole-area deposition of SiO₂ with subsequent planarization is preferably carried out.

Finally, as in the first exemplary embodiment, phase change memory elements PW1 and PW2 may once again be formed at the locations of the uncovered nanoelements **9** or at the surface of the auxiliary dielectric layer **22**, the memory device being completed in accordance with the third exemplary embodiment.

Once again, a memory device with a maximum integration density in which contact-connection is formed essentially in a self-aligning manner is obtained, in accordance with FIG. **16A**.

FIG. **16B** shows a simplified plan view with a sectional illustration A-A of the sectional view illustrated in FIG. **16A** in order to illustrate this third exemplary embodiment.

In accordance with this third exemplary embodiment, it is consequently possible to employ a so-called dual damascene bit line process, which enables the costs to be reduced further. It goes without saying that further additional hard masks can also be used in accordance with the third exemplary embodiment.

The present invention has been described on the basis of phase change memory elements and capacitors as memory

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elements. However, it is not restricted thereto and also encompasses alternative memory elements in the same way. Furthermore, the invention has been described on the basis of two one-transistor memory cells in which two selection transistors are formed in an active region. However, it is not restricted thereto and also encompasses other types of memory cells in the same way.

As a person skilled in the art will readily appreciate, the above description is meant as an illustration of implementation of the principles this invention. This description is not intended to limit the scope or application of this invention in that the invention is susceptible to modification, variation and change, without departing from the spirit of this invention, as defined in the following claims.

We claim:

1. A memory device comprising:

a semiconductor substrate having insular active regions;
at least one memory element formed on each insular active region for storing items of information; and

at least one selection transistor formed on each insular active region for selecting the at least one memory element via at least one word line and for reading/writing the information via at least one bit line connected to the at least one memory element via the at least one selection transistor,

wherein an electrically conductive nanoelement connects the memory element to the selection transistor and the entire bit line is embedded in a dielectric layer of the memory device;

wherein the nanoelement is connected to the selection transistor via a metal-semiconductor compound material; and

wherein the source/drain regions are defined in a self-aligned manner in respective insular active regions by means of at least one word line which divides the respective insular active regions into at least two partial regions with regard to a plan view, and wherein a first insular active region divided by one or more first word lines overlaps a second insular active region divided by one or

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more second word lines which are different from the one or more first word lines in a view along a direction of the first and second word lines.

2. The memory device as claimed in claim 1, wherein the nanoelement includes a nanowire, a nanotube or a nanofiber.

3. The memory device as claimed in claim 1, wherein the nanoelement has fully silicided silicon.

4. The memory device as claimed in claim 1, wherein the selection transistor includes a field effect transistor having source and drain regions formed in the respective active regions of the semiconductor substrate and serving for defining a channel, a gate dielectric layer formed on the channel, and a gate layer formed on the gate dielectric layer, the nanoelement being formed in a self-aligned manner on at least one source and/or drain region.

5. The memory device as claimed in claim 4, wherein the source and drain regions have elevated semiconductor layers that are deposited epitaxially on the semiconductor substrate.

6. The memory device as claimed in claim 4, wherein the metal semi-semiconductor compound material comprises metal-semiconductor compound layers formed on the source and drain regions.

7. The memory device as claimed in claim 1, wherein a bit line layer for realizing the bit line is connected to the selection transistor via a further nanoelement.

8. The memory device as claimed in claim 1, wherein a bit line layer for realizing the bit line is directly connected to the selection transistor.

9. The memory device as claimed in claim 1, wherein the memory element includes a volatile or nonvolatile capacitor.

10. The memory device as claimed in claim 1, wherein the memory element includes a phase change memory element.

11. The memory device as claimed in claim 1, wherein the memory element includes an MRAM or CBRAM memory element.

12. The memory device as claimed in claim 1, wherein two selection transistors with two memory elements are formed on the respective insular active regions, which are electrically connected via a common drain region of the selection transistors.

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